AF/2665 #1

Docket No.: 64965-134

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of	:	Customer Number: 20277
Jeffrey DWORK	:	Confirmation Number: 5785
Serial No.: 09/505,062	:	Group Art Unit: 2665
Filed: February 16, 2000	:	Examiner: Thien D. Tran

For: METHOD AND APPARATUS FOR AUTOPOLLING PHYSICAL LAYER DEVICES IN A NETWORK

REQUEST FOR REINSTATEMENT OF THE APPEAL UNDER 37 CFR 1.193(b)(2)

Mail Stop Appeal Brief-Patents
Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

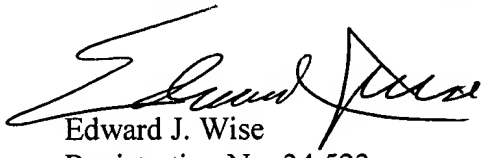
This Request is submitted pursuant to 37 CFR 1.193(b)(2) in response to reopening of prosecution in the Office Action mailed May 5, 2004.

Reinstatement of the Appeal filed on December 11, 2003 is respectfully requested. Submitted herewith in triplicate is Appellant's Supplemental Appeal Brief. Appeal Brief fee was paid on December 11, 2003.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension-of-time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



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For: METHOD AND APPARATUS FOR AUTOPOLLING PHYSICAL LAYER DEVICES IN A NETWORK

TRANSMITTAL OF SUPPLEMENTAL APPEAL BRIEF

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith in triplicate is Appellant's Supplemental Appeal Brief in support of the Request for Reinstatement of the Appeal Under 37 CFR 1.193(b)(2) filed concurrently herewith.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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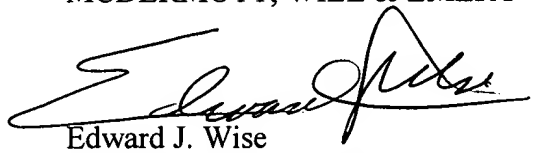

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For: METHOD AND APPARATUS FOR AUTOPOLLING PHYSICAL LAYER DEVICES IN A NETWORK

SUPPLEMENTAL APPEAL BRIEF

Mail Stop Appeal Brief-Patents
Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Supplemental Brief is submitted pursuant to the rejection of claims 1-7 and 13-15 in the Official Action dated May 5, 2004, and is submitted concurrently with the submission of a request to reinstate the appeal.

STATUS OF CLAIMS

In response to the Appeal Brief date February 11, 2004, the Examiner reopened prosecution and issued a non-final Office Action dated May 5, 2004, rejecting claims 1-7 and 13-15, and indicating that claims 8-12 and 16-19 were objected to, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. However, these claims have not been amended to be in independent form at this time.

STATUS OF AMENDMENTS

No Amendment has been filed after the Official Action dated May 5, 2004.

ISSUES

1. Whether claims 1-7 and 13-15 are unpatentable under 35 U.S.C. § 103 for obviousness predicated upon Booth (U.S. Patent No. 6,065,073) in view of Kelley, Jr. [et al.] Booth (U.S. Patent No. 64,751,630).

GROUPING OF CLAIMS

As to the grounds of rejection of claims 1-7 and 13-15, the rejected claims do not stand or fall together as a single group. Claims 1-4 stand or fall together as a group. Claims 5-7 each stand alone and will be separately argued. Claims 11-12 stand or fall together as a group. Claim 13 stands alone and will be argued separately and claims 14 and 15 stand or fall together as a group.

REJECTION

Claims 1-7 and 13-15 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Booth in view of Kelley, Jr. [et al.]. The Examiner contends that Booth discloses the claimed invention except for "a number (n) of poll registers that store information indicating which PHY registers are to be polled. However, it would have been obvious to one having ordinary skill in the art to have the number of poll registers used for an indication of which PHY register [is] being polled so that a selective NIC can be chosen for processing due to an interrupt signal. For example, Kelley discloses addresses of polling list terminals stored in registers for the lookup of specific addresses to be polled, col. 6, lines 35-45. Therefore, the overall system performance is effectively achieved."

THE REFERENCES

As noted in the Appeal Brief dated February 11, 2004, Booth discloses an auto polling unit for interrupt generation in a network interface device and depicts the auto polling unit 920 in Fig. 11. The description of the auto polling unit 920 is provided in columns 19 and 20.

The auto polling unit 920 includes a host CPU data register 914, an auto poll data register 916A, an auto poll hold data register 916B, an auto poll control unit 919, an interrupt status data multiplexer 922, and a comparator 912. The operation of the auto polling unit 920 is governed according to an auto polling state machine described in Fig. 12.

When the host CPU 202 begins writing a PHY, the auto polling unit 920 is able to determine the ***address of the PHY device*** that it will eventually poll. However, auto-polling does not being until the PHY is valid. When a PHY is valid, auto-polling control unit 918 beings monitoring activity on the management interface of the currently selected PHY. This monitoring continues until a counter timeout is detected whereupon, an auto-poll read operation is performed. Referring now to column 20, lines 4-53, the auto-poll read operation involves auto polling unit 920 accessing a status register 944 of a currently selected PHY device via a management interface. The value read from the status register 944 of the currently selected PHY device is conveyed to the auto poll registers 916A-B via management interface logic unit 930. The contents of the auto poll data register 916A are then conveyed to comparator 912, which also receives the contents of host CPU data register 914. After the auto poll read, comparator 912 performs a comparison of the current status value from register 916A and the most recent status value read by the host CPU. If there is a mismatch detected between the two values, an interrupt to the host CPU is generated. The host CPU responds to the assertion of the interrupt signal by requesting a read of the status register data which caused the interrupt. This data is

conveyed to the host CPU from the auto poll hold data register 916B. The read request by the CPU also causes the registers 914 and 916A to update the same value to de-assert the interrupt signal 924. The de-assertion of the interrupt signal causes the state machine to transition to reset the counter time out and return to the monitoring state. In this manner, auto-polling is disabled while interrupt signal 924 is asserted.

Kelley, Jr. [et al.] relates generally to an interactive terminal system wherein information is transferred between a communications controller and a number of work stations over a single line, and relates more particularly to the prepolling of a work station prior to the communications controller transferring a block of information to the work station.

ARGUMENTS

A. The rejection of claims 1-4 under 35 U.S.C. § 103(a) as being unpatentable over Booth in view of Kelley, Jr. [et al.] is improper since the Examiner has failed to fulfill the initial burden of identifying a source in the applied prior art for the claim limitations.

The Examiner is charged with the initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention under any statutory provision. ***In re Mayne***, 104 F.3d 1339, 41 USPQ2d 1451 (Fed. Cir. 1997). In rejecting a claim under 35 U.S.C. § 103, the Examiner is required to identify a source in the applied prior art for: (1) every claim limitation; and (2) the requisite motivation for combining applied references with a reasonable expectation of achieving a particular benefit. ***Smith Industries Medical Systems v. Vital Signs***, 183 F.3d 1347, 51 USPQ2d 1415 (Fed. Cir. 1999).

Claim 1 requires an arrangement for polling PHY registers in the network, comprising a number of poll registers that store information indicating which PHY registers are to be polled. The

arrangement also comprises a number of poll data registers that receive polled information from the PHY registers. The poll logic automatically polls those PHY registers indicated by the information in the poll registers as PHY registers to be polled, and stores the polled information in the PHY registers.

In the Official Action of May 5, 2004, the Examiner admits that Booth does not disclose a number (n) of poll registers that store information indicating which PHY registers are to be polled. The Examiner refers to col. 6 lines 35-45 of Kelley, Jr. [et al.] as disclosing addresses of polling list terminals stored in registers for lookup of specific addresses to be polled. However, col. 6, lines 35-47 of Kelley, Jr. [et al.] describe:

> The HSLC 12 contains three types of registers: registers that interface to the system bus 2, registers that interface to the HSLC 12 data bus 35, and registers that interface with both the system bus 2 and HSLC 12 data bus 35 and address bus 32.
>
> In response to a command from CPU 4 for the HSLC 12 identification code, the HSLC 12 sends the output signals D0 through D7 of a link ID 64 over data bus 34 to CPU 4. This allows CPU 4 to verify the identify of the HSLC 12 during the system initialization operation.
>
> A control logic 69 receives address signals A0 through A3 from the CPU 4 via address bus 32 to generate a number of signals.

Nothing in this section describes addresses of polling list terminals stored in registers for lookup of specific addresses to be polled. Furthermore, the description that control logic 69 receives address signals A0 through A3 from the CPU 4 via address bus 32 to generate a number of signals appears to support the fact that address for polling are generated by CPU 4. Even if it were presumed that CPU has a list for polling, the use of CPU 4 to generate the addresses may prove antithetic to performing auto-polling in Booth, which strives, as does the present invention, to provide a more efficient use of system resources, particularly CPU bandwidth since the CPU does not have to waste bandwidth by continually polling network interface devices (column 8, lines 40-45 of Booth).

Furthermore, even if Kelley, Jr. [et al.] is presumed to disclose addresses of polling list terminals stored in registers for lookup of specific addresses to be polled, the "terminals" referred to in

Booth are the individual work stations 16-1 through 16-48. Reasonable interpretation of the disclosure in Kelley, Jr. [et al.] evince that such work stations correspond to each PHY, not to PHY ***registers*** (in each PHY) that are to be polled.

As noted in the Appeal Brief dated February 11, 2004, PHY devices may have a number of registers, as depicted in Fig. 3 of the present specification. For example, a single PHY device 62 may contain six different PHY registers 76. Both Booth and Kelley, Jr. [et al.] fail entirely to show poll registers that store information indicating which PHY ***registers*** are to be polled.

Since claim 1 of the present invention requires a number of poll ***registers*** that store information indicating which PHY **registers** are to be polled, and Booth and Kelley, Jr. [et al.] both fail to disclose such a feature, the Examiner has not discharge the initial burden of identifying wherein Booth and Kelley, Jr. [et al.] disclose or suggest: a number of poll registers that store information indicating which PHY registers are to be polled. Consequently, the rejection of independent claim 1 and those claims dependent there from under 35 U.S.C. § 103(a) should not be sustained.

B. The rejection of claims 5-7 under 35 U.S.C. § 103(a) as being unpatentable over Booth in view of Kelley, Jr. [et al.] is improper since the Examiner has failed to fulfill the initial burden of identifying a source in the applied prior art for the claim limitations.

Claim 5 of the present invention requires that that n = m, where the number n is the number of poll registers that store information indicating which PHY registers are to be polled and the number m is the number of polled data registers that receive polled information from the PHY registers. The Examiner asserts "Regarding claim 5, Booth discloses that n and m are any integer. See col. 8, lines 5-20." Column 8, lines 1-21 of Booth describe:

> The present invention also comprises a system and method for monitoring a currently established network link. In prior art systems, a host CPU in a computer system

> is required to continually poll a register in a network interface card in order to test the status of the currently established link. This has the disadvantage of becoming a drain on the bandwidth of the host CPU, particularly if the polling does not frequently result in retrieval of updated status values. This decrease in bandwidth adversely affects system performance.
>
> In one embodiment, the present invention includes a system for auto-polling to determine the current link status. This system includes a host CPU and a network interface card (NIC), wherein the NIC includes, a physical layer device and an auto-polling unit. The physical layer interface device is coupled to a network via a first transmission medium. Control values for this device may be changed via a management interface (such as the MDIO/MDC interface defined by IEEE standard 802.3u, clause 22). Status values for the device are included within a designated status register.

Clearly, there is nothing in this section regarding that n and m are any integer where (n) is the number of poll registers that store information indicating which PHY registers are to be polled and (m) is a number of poll data registers that receive polled information from the PHY registers. Furthermore, even if it were presumed that Booth discloses that n and m are any integer, this clearly does not establish that n = m.

Clearly, the Examiner has not discharge the initial burden of identifying wherein Booth and Kelley, Jr. [et al.] disclose or suggest: that n = m.

Claim 6 requires that each of the poll registers includes an address field that contains an address of a PHY containing a PHY register to be polled. However, as noted in the Appeal Brief dated February 11, 2004, the Examiner has failed to establish that Booth discloses poll registers whatsoever. The Examiner refers to column 5, lines 45-65 of Booth. This portion of Booth refers to the prior art and not to any poll registers alleged by the Examiner to be present in the Booth embodiment described in Fig. 11. Further, the suited portion of Booth does not describe an address field that contains an address of a PHY containing a PHY register to be polled. Therefore, Booth fails to disclose the limitation recited in claim 6.

Clearly, the Examiner has not discharge the initial burden of identifying wherein Booth and Kelley, Jr. [et al.] disclose or suggest: that each of the poll registers includes an address field that contains an address of a PHY containing a PHY register to be polled.

Claim 7 requires that each of the poll registers includes a **register number field** that contains a register number of the PHY register to be polled of the PHY indicated by the address contained in the address field. In addition to Booth failing to disclose poll registers as claimed in the present invention, Booth also fails to disclose that these poll registers include a register number field. Col. 7, lines 20-55 of Booth does not describe any such register number field. The Examiner is reminded that merely citing a large portion of text does not provide the particularity that shows which element of Booth corresponds to the register number field claimed in the present invention.

Clearly, the Examiner has not discharge the initial burden of identifying wherein Booth and Kelley, Jr. [et al.] disclose or suggest: that each of the poll registers includes a **register number field** that contains a register number of the PHY register to be polled of the PHY indicated by the address contained in the address field.

C. The rejection of claims 13-15 under 35 U.S.C. § 103(a) as being unpatentable over Booth in view of Kelley, Jr. [et al.] is improper since the Examiner has failed to fulfill the initial burden of identifying a source in the applied prior art for the claim limitations.

Independent claim 13 relates to a method of automatically polling PHY registers of a network and comprises the steps of storing addresses of a subset of PHY registers from a plurality of PHY registers, periodically polling the PHY registers whose addresses are stored and storing polling results obtained by the periodic polling. The polling results are compared with previous polling results and an interrupt signal is generated when the polling results are different from the previous polling results.

The Examiner, in making his rejection, admits that "Booth does not disclose the storing address of a subset of PHY registers from a plurality of PHY registers. However, Booth discloses that addresses of PHY registers being retrieved by the auto-polling unit for polling, col. 19 lines 55-65. Therefore, it would be obvious to one having ordinary skill in the art to have addresses of PHY registers stored at a memory or registers so that the locations of PHY registers can be identified properly by the polling unit for processing".

With regard to the rejection of independent claim 13, the Examiner fails to state what (feature) is not disclosed in Booth that is disclosed in Kelley, Jr [et al.] and to explain how and why one having ordinary skill in the art would have been led to modify the system of Booth in view of the disclosure/teaching of Kelley, Jr. [et al.] to arrive at the claimed invention. Consequently, the inclusion of Kelley, Jr. [et al.] in the statement of rejection of claim 13 is improper.

Column 19, line 45 though column 20, line 2 of Booth (referred to by the Examiner) describes:

> FIGS. 12-13--Operation of Auto-polling unit
>
> Referring now to FIG. 12, a state machine 1000 is depicted which describes operation of auto-polling unit 920 shown in FIG. 11. The start state of state machine is 1002, in which the auto-polling feature is disabled. State machine 1000 remains in state 1002 until such time as auto-polling is enabled by host CPU 202 (causing a transition to state 1004).
>
> State machine 1000 remains in state 1004 until host CPU 202 performs one or more writes which cause a particular PHY to become active. (Specifically, these writes remove the PHY from reset, power-down, and isolation modes). When host CPU 202 begins writing a PHY, auto-polling unit 920 is able to determine the address of the PHY device that it will eventually poll. Auto-polling does not begin, however, until the PHY is valid.
>
> When a PHY is valid, state machine 1000 transitions to state 1006. Auto-polling control unit 918 begins monitoring activity on the management interface of the currently selected PHY. The state machine remains in state 1006 until a counter timeout is detected. In a preferred embodiment of the invention, this counter timeout corresponds to 32 clock cycles on MDC 932 during which there is no activity on MDIO 934.

Thus, this portion describes that when the host CPU 202 begins writing a PHY, the auto polling unit 920 is able to determine the address of the PHY device that it will eventually poll. It does not

state, however, that the arrangement of Booth stores addresses of a subset of PHY registers from a plurality of PHY registers. Nor does it disclose the periodic polling of the PHY registers whose addresses are stored. The Examiner has not been able to show wherein Booth the storing of addresses of PHY registers is clearly disclosed. The best that can be said that is taught in this section of Booth is that the address of the PHY device to which the CPU 202 begins writing will be used by auto polling 920 as the address of the PHY device that it will eventually poll (after the writing). This is clearly different from what is recited in claim 13.

Clearly, the Examiner has not discharge the initial burden of identifying wherein Booth and Kelley, Jr. [et al.] disclose or suggest: storing addresses of a subset of PHY registers from a plurality of PHY registers; (and) periodically polling of the PHY registers whose addresses are stored.

Claim 14 requires the addresses of the PHY registers to be stored in poll registers. The Examiner refers to column 19, lines 45-67 of Booth as disclosing this feature. Column 19, lines 45-67 of Booth are described above. As previously noted, this portion describes that when the host CPU 202 begins writing a PHY, the auto polling unit 920 is able to determine the address of the PHY device that it will eventually poll. Consequently, the best that can be said is that this portion describes is that the address of the PHY (to which the CPU 202 has just written to) will be the address of the PHY to be polled. This portion clearly does not establish that Booth discloses the storing of addresses of PHY ***registers*** (to be polled) in poll registers.

Clearly, the Examiner has not discharge the initial burden of identifying wherein Booth and Kelley, Jr. [et al.] disclose or suggest: that the addresses of the PHY registers are stored in poll registers.

Claim 15 depends from claim 14 and should be considered patentable over Booth and Kelly, Jr. [et al.] for the same reason that claim 14 is patentable over these references.

CONCLUSION

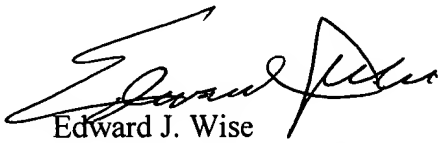
For the reasons advanced above, Appellant respectfully urges that the rejection of claims 1-7 and 13-15 as being unpatentable under 35 U.S.C. § 103 for obviousness predicated upon Booth in view of Kelley, Jr. [et al.] should not be sustained as the Examiner has not established a *prima facie* case of obviousness.

PRAYER FOR RELIEF

Based upon the above arguments, Appellant submits that one having ordinary skill in the art would not have found the claimed invention as a whole obvious within the meaning of 35 U.S.C. § 103. Appellant, therefore, respectfully solicit the Honorable Board to reverse the Examiner's rejection of claims 1-7 and 13-15 under 35 U.S.C. § 103 for obviousness predicated upon Booth in view of Kelley, Jr. [et al.].

Respectfully submitted,

MCDERMOTT, WILL & EMERY



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APPENDIX

1. An arrangement for polling external physical layer device (PHY) registers in a network, comprising:

a number (n) of poll registers that store information indicating which PHY registers are to be polled;

a number (m) of poll data registers that receive polled information from the PHY registers; and

poll logic that automatically polls those PHY registers indicated by the information in the poll registers as PHY registers to be polled, and stores the polled information in the PHY registers.

2. The arrangement of Claim 1, wherein the poll logic includes comparison logic that compares currently polled information with previously polled information stored in the poll data registers.

3. The arrangement of Claim 2, wherein the poll logic includes write logic responsive to the comparison logic to replace the previously polled information stored in the poll data registers with the currently polled information when the currently polled information is different than the previously polled information.

4. The arrangement of Claim 3, wherein the poll logic includes interrupt generation logic responsive to the comparison logic to generate an interrupt signal when the currently polled information is different than the previously polled information.

5. The arrangement of Claim 1, wherein n=m.

6. The arrangement of Claim 1, wherein each of the poll registers includes an address field that contains an address of a PHY containing a PHY register to be polled.

7. The arrangement of Claim 6, wherein each of the poll registers includes a register number field that contains the register number of the PHY register to be polled of the PHY indicated by the address contained in the address field.

8. (Objected To) The arrangement of Claim 7, wherein each of the poll registers includes an enable field that enables and disables automatic polling of the PHY register to be polled.

9. (Objected To) The arrangement of Claim 8, where, in one of the poll registers, the enable field is always set to enable automatic polling, the register number is set to the status register of the PHY, and the address field contains the address of a default PHY.

10. (Objected To) The arrangement of Claim 9, wherein each of the poll registers includes a preamble suppression field that contain information which determines whether the poll logic is to send management frames to the PHY registers without preambles.

11. (Objected To) The arrangement of Claim 10, wherein each of the poll registers includes a default field that contains information which determines whether the address in the address field is to be used or the address of the default PHY is to be used to determine the PHY register to be polled.

12. (Objected To) The arrangement of Claim 11, wherein the poll logic is configured to suppress a preamble when the default PHY accepts management frames with no preamble.

13. A method of automatically polling physical layer device (PHY) registers of a network, comprising the steps of:

storing addresses of a subset of PHY registers from a plurality of PHY registers; periodically polling the PHY registers whose addresses are stored;

storing polling results obtained by the periodically polling;

comparing the polling results with previous polling results; and

generating an interrupt signal when the polling results are different from the previous polling results.

14. The method of Claim 13, wherein the addresses of the PHY registers are stored in poll registers.

15. The method of Claim 14, wherein the polling results are stored in poll data registers.

16. (Objected To) The method of Claim 15, further comprising enabling and disabling the periodic polling by setting and clearing an enable field in the poll registers.

17. (Objected To) The method of Claim 16, further comprising setting the enable field of one of the poll registers to permanently enable periodic polling, and storing the address of a status register of a default PHY in an address field of that poll register.

18. (Objected To) The method of Claim 17, further comprising sending management frames without preambles to PHY registers in dependence on the setting of a preamble suppression field in the poll registers.

19. (Objected To) The method of Claim 18, further comprising setting a default field in the poll registers to control whether the address stored in the poll register is to be used as the address of the default PHY when a PHY register is polled.